

FIG. 1

The diagram illustrates a 6-bit digital-to-analog converter (DAC) circuit for an LCD. The circuit is composed of several key blocks and components:

- Charge Pumps (CHP):**
  - CHP1 (Vccx6):** Powered by  $V_{cc}$  and  $clk$ , it outputs  $V_{out1}$  to capacitor  $C1$ .
  - CHP2 (V0-Vccx2):** Powered by  $V_0$  and  $V_{cc}$ , it outputs  $V_{out2}$  to capacitor  $C2$ .
  - CHP3 (Vccx2):** Powered by  $V_0$  and  $V_{cc}$ , it outputs  $V_{out3}$  to capacitor  $C3$ .
- Resistor Network:** A series of resistors  $R0, R1, R2, R3, R4$  are connected between the output nodes  $V_{out1}, V_{out2}, V_{out3}$  and the data lines  $V0r, V1r, V2r, V3r, V4r$ .
- Inverters:**
  - A1 (xn):** An inverter with gain  $xn$  connected between  $V_{out1}$  and  $V0r$ .
  - B0, B1, B2, B3, B4:** A chain of inverters connected between the data lines  $V0, V1, V2, V3, V4$  and the nodes  $V0r, V1r, V2r, V3r, V4r$ .
- Reference Voltage:** A reference voltage  $V_{ref}$  is applied to the input of inverter A1.
- LCD:** The LCD is connected to the data lines  $V0, V1, V2, V3, V4, V5$  and a common line  $V0$ .

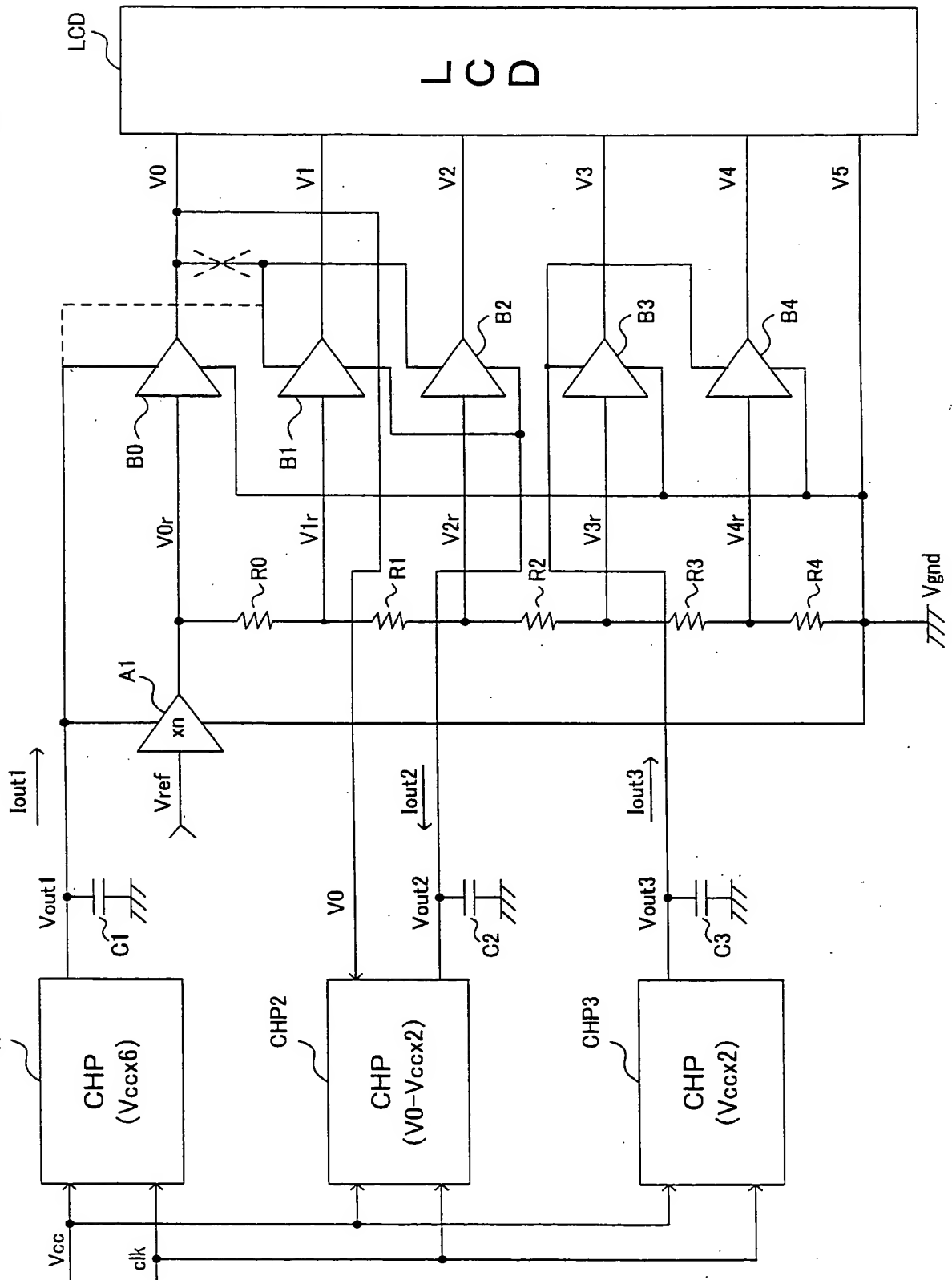


FIG. 2 A

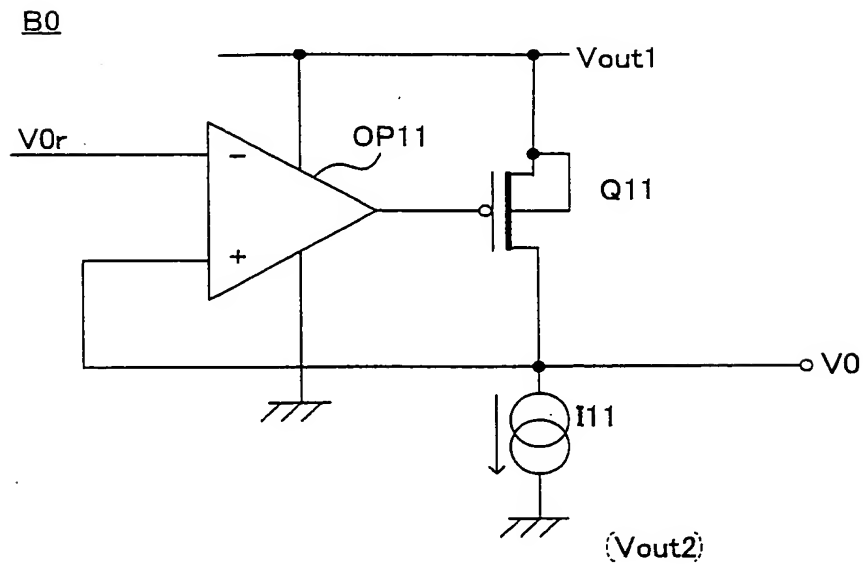


FIG. 2 B

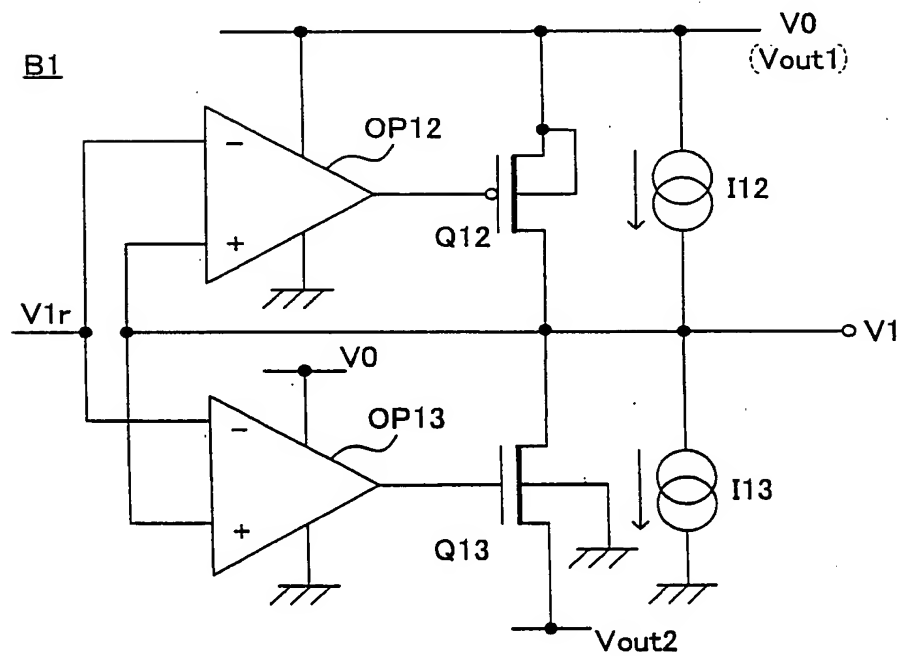


FIG. 2 C

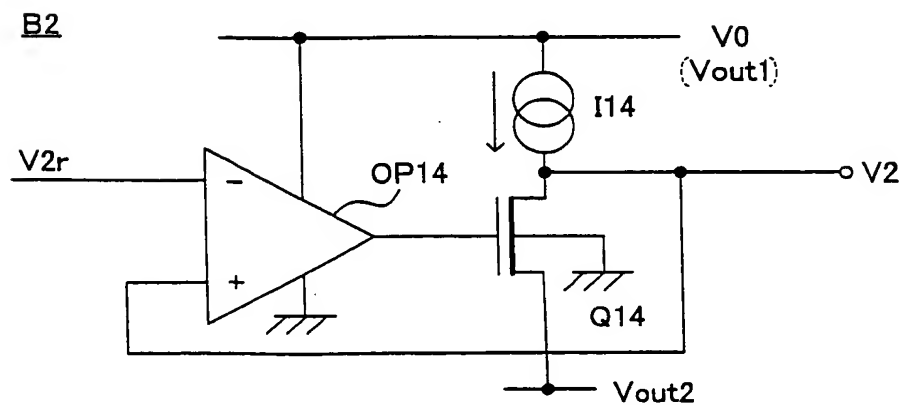


FIG. 3 A

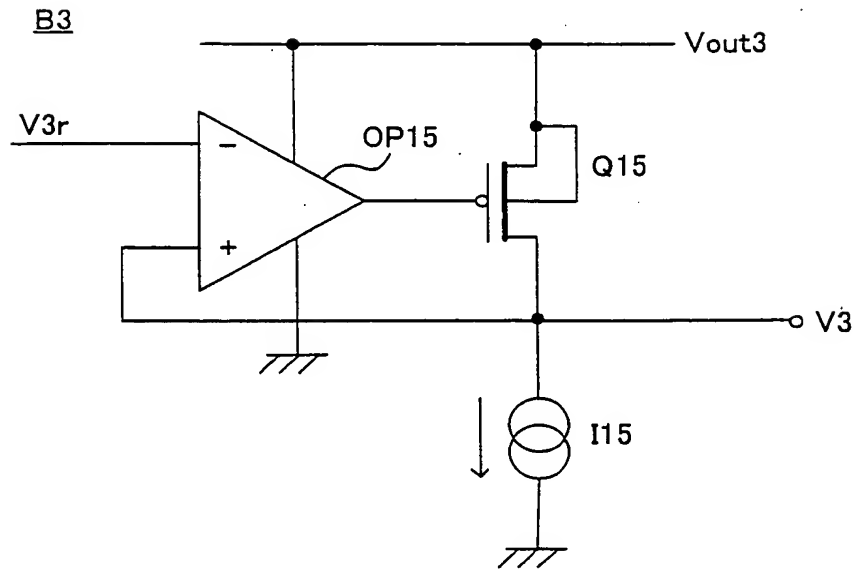


FIG. 3 B

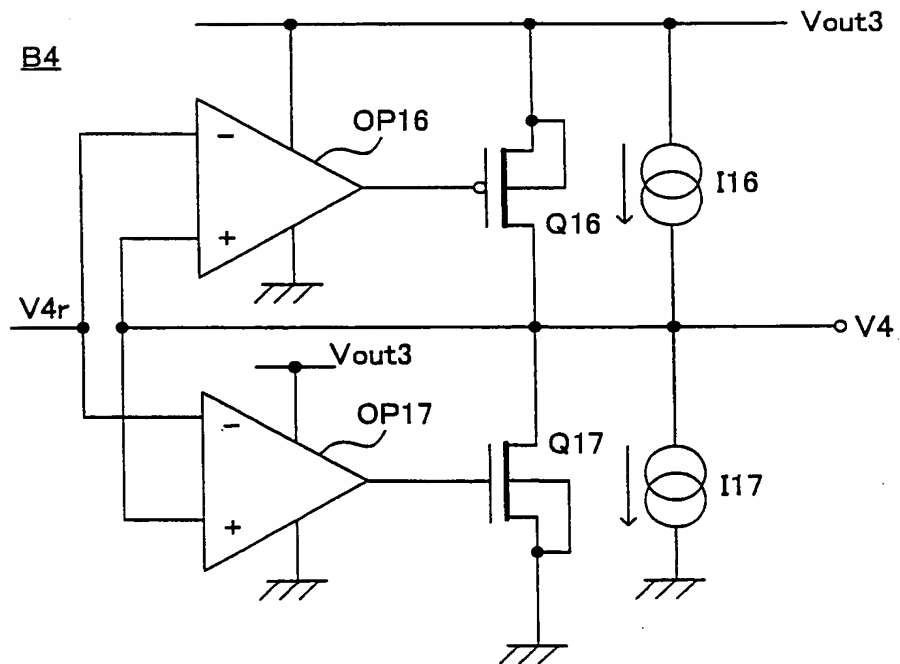


FIG. 4

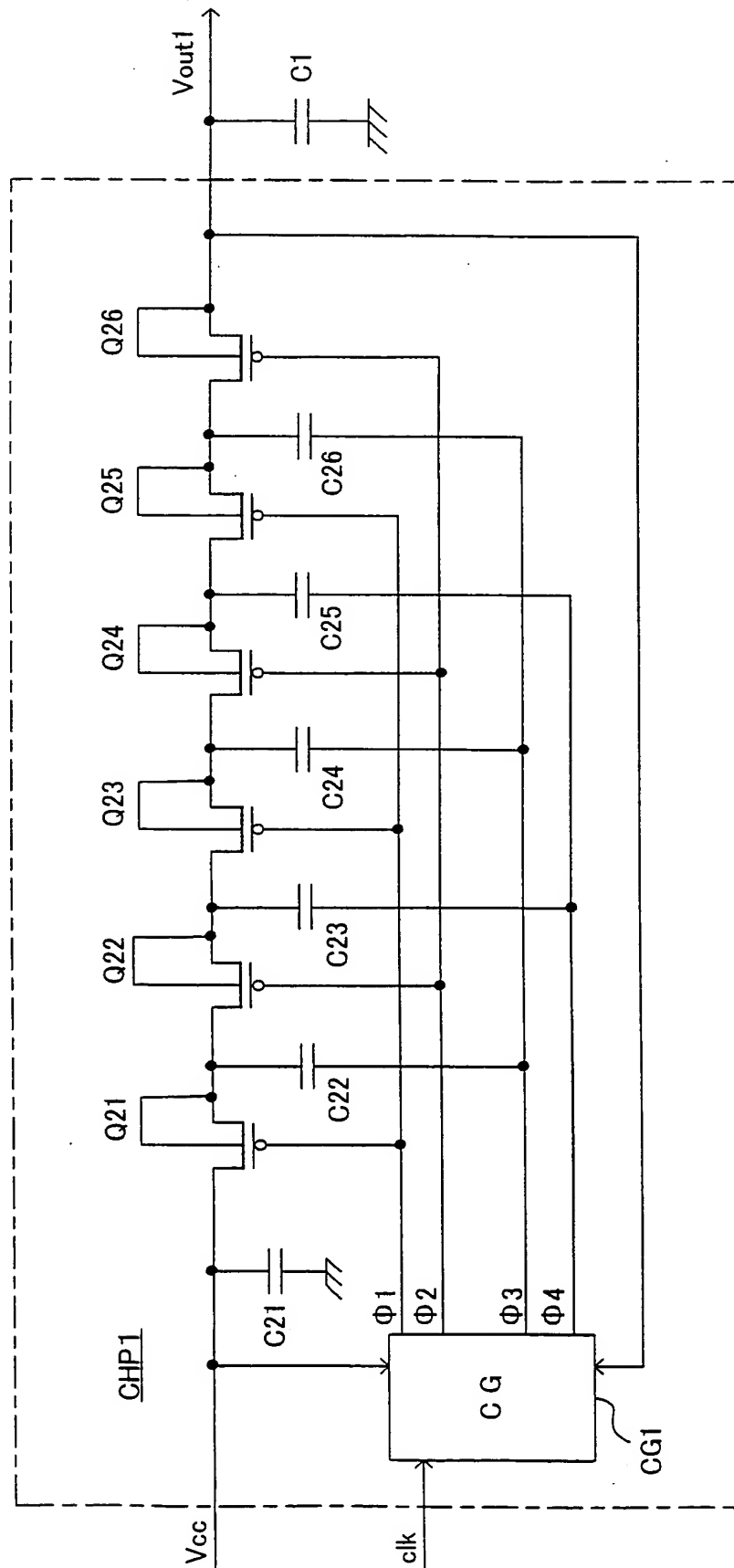


FIG. 5

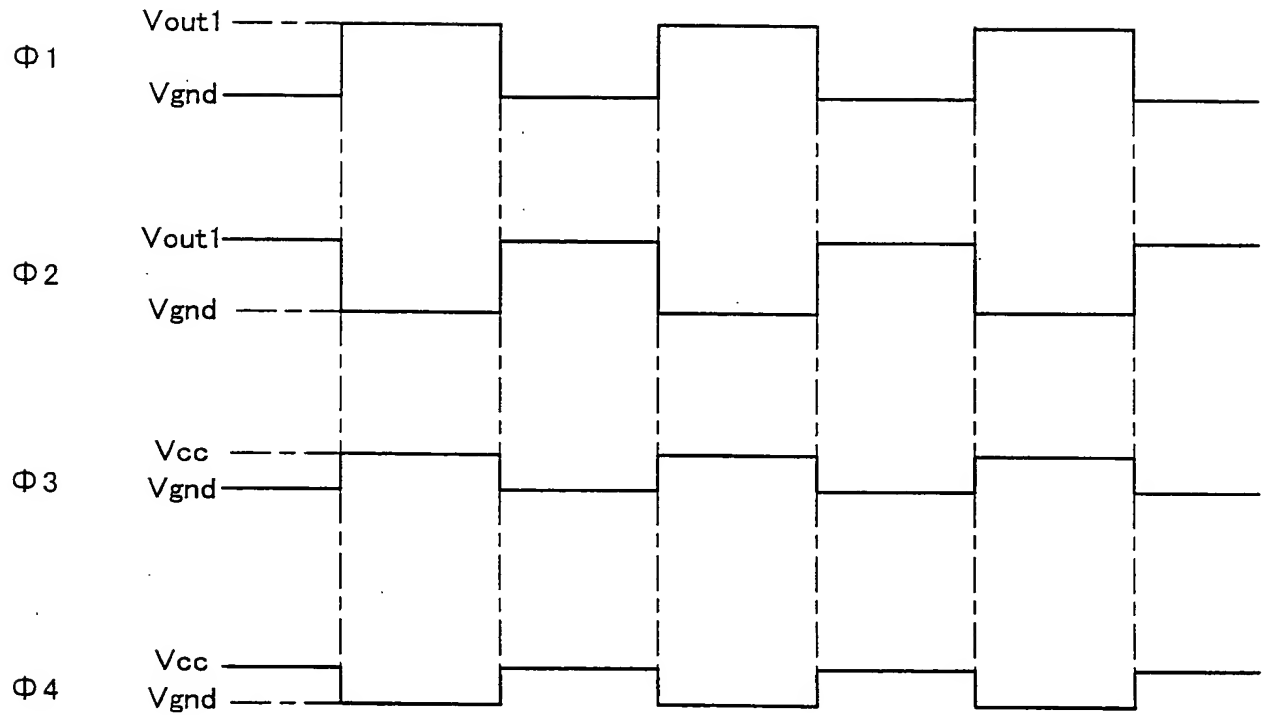


FIG. 6

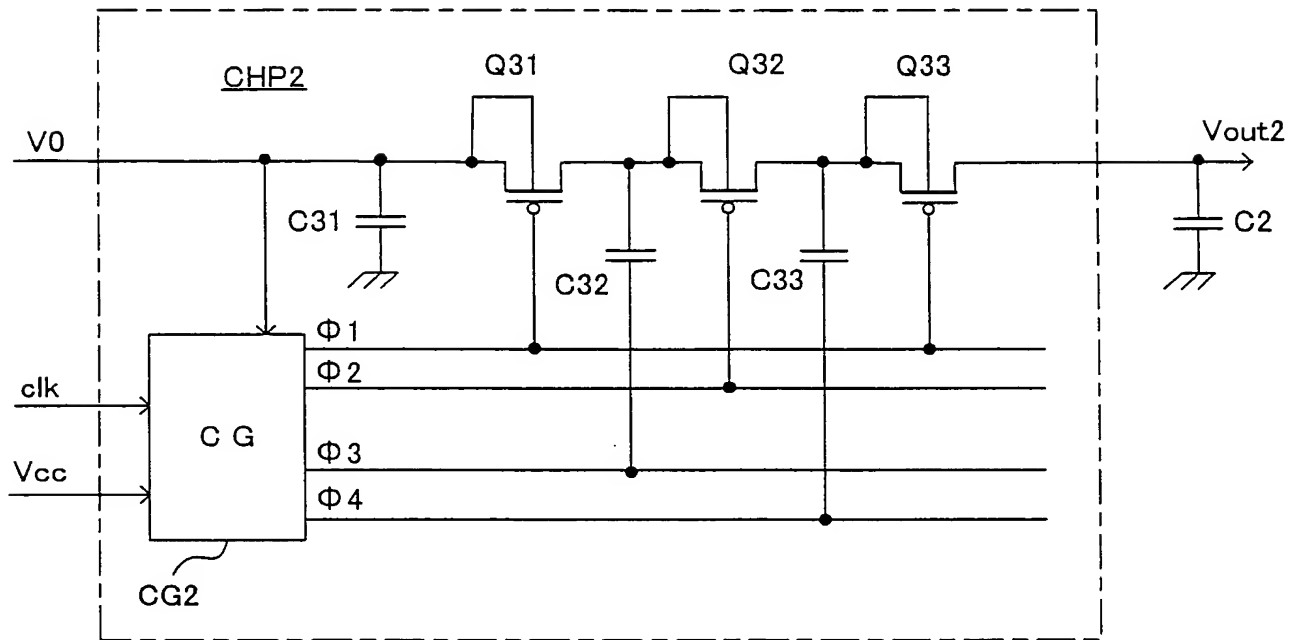


FIG. 7

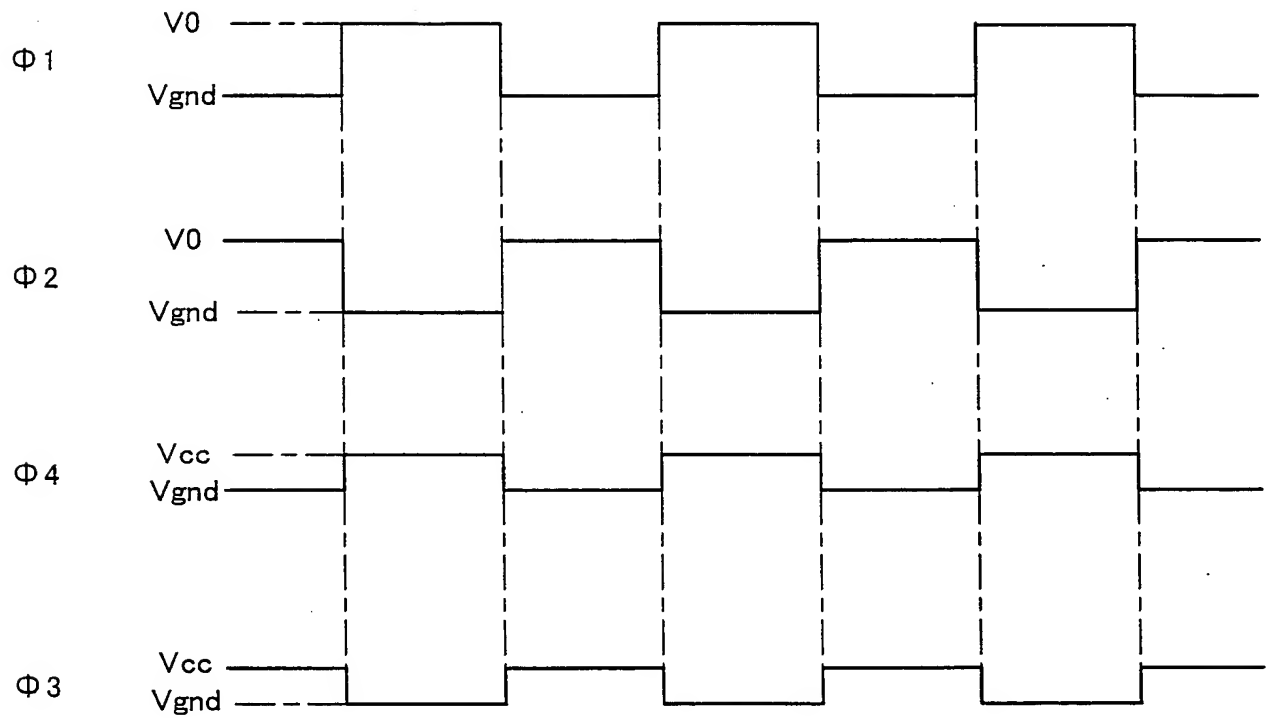


FIG. 8

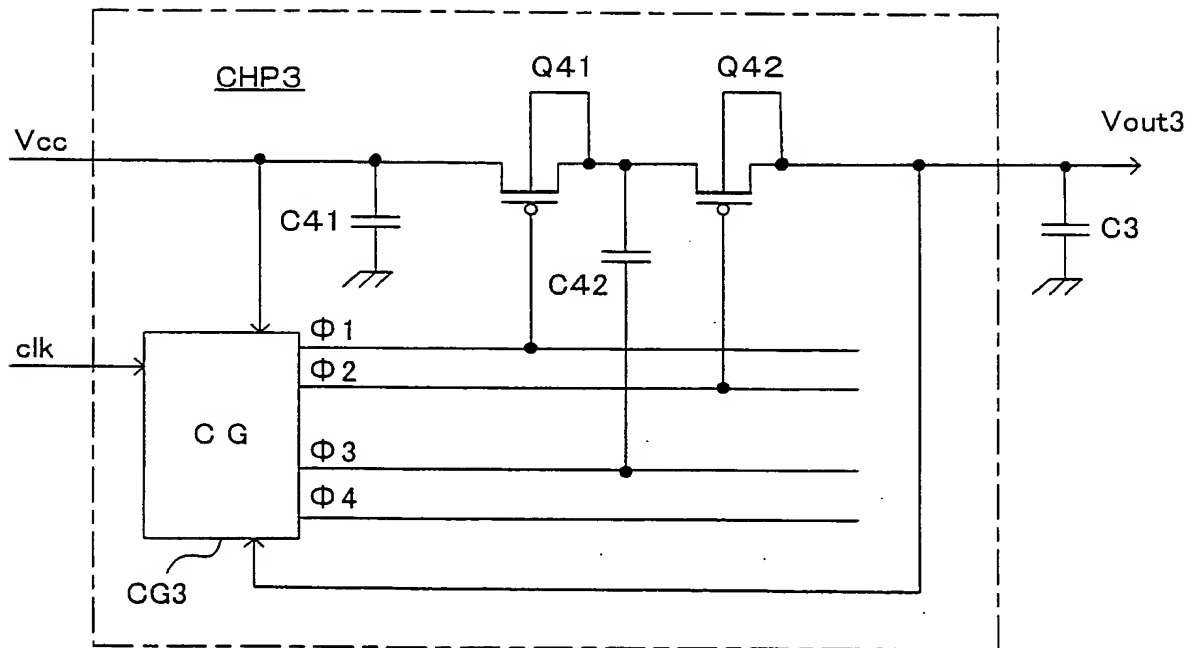




FIG. 9

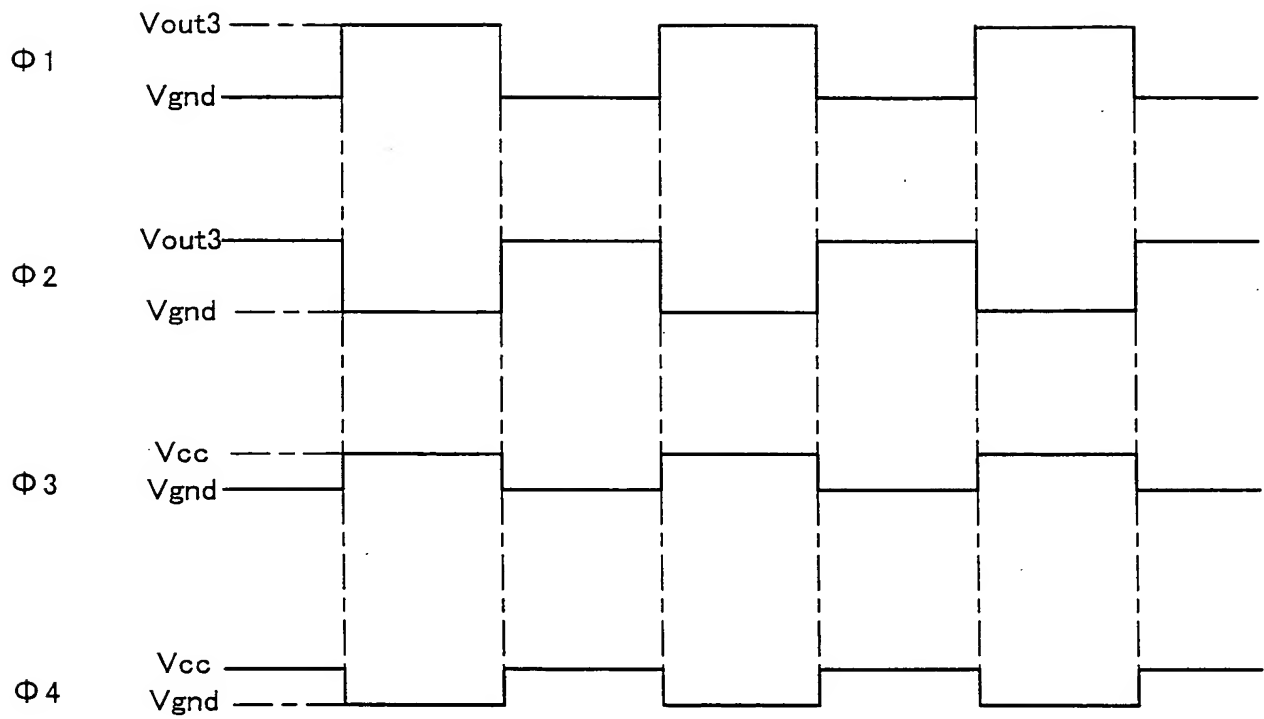


FIG. 10

The diagram illustrates a 6-bit digital-to-analog converter (DAC) circuit. It features a feedback loop with an inverting operational amplifier (A1) and a summing junction. The feedback signal is derived from the output of a current mirror array (B0-B4) and is fed back to the inverting input of A1. The current mirror array consists of five stages, each with a PMOS transistor (B0-B4) and a resistor (R0-R4). The input signals V0-V5 are applied to the gates of the PMOS transistors. The output of the current mirror array is connected to the summing junction of A1. The feedback signal is also connected to the non-inverting input of A1. The output of A1 is connected to the gates of the PMOS transistors. The output of the DAC is connected to the gates of the PMOS transistors. The circuit is powered by Vcc and Vgnd. The output of the DAC is connected to the gates of the PMOS transistors. The circuit is labeled with various components and signals, including V0, V1, V2, V3, V4, V5, V0r, V1r, V2r, V3r, V4r, Vgnd, R0, R1, R2, R3, R4, B0, B1, B2, B3, B4, A1, Vref, Vout1, Vout2, Vout3, C1, C2, C3, CHP1A, CHP2A, CHP3A, and CLK.

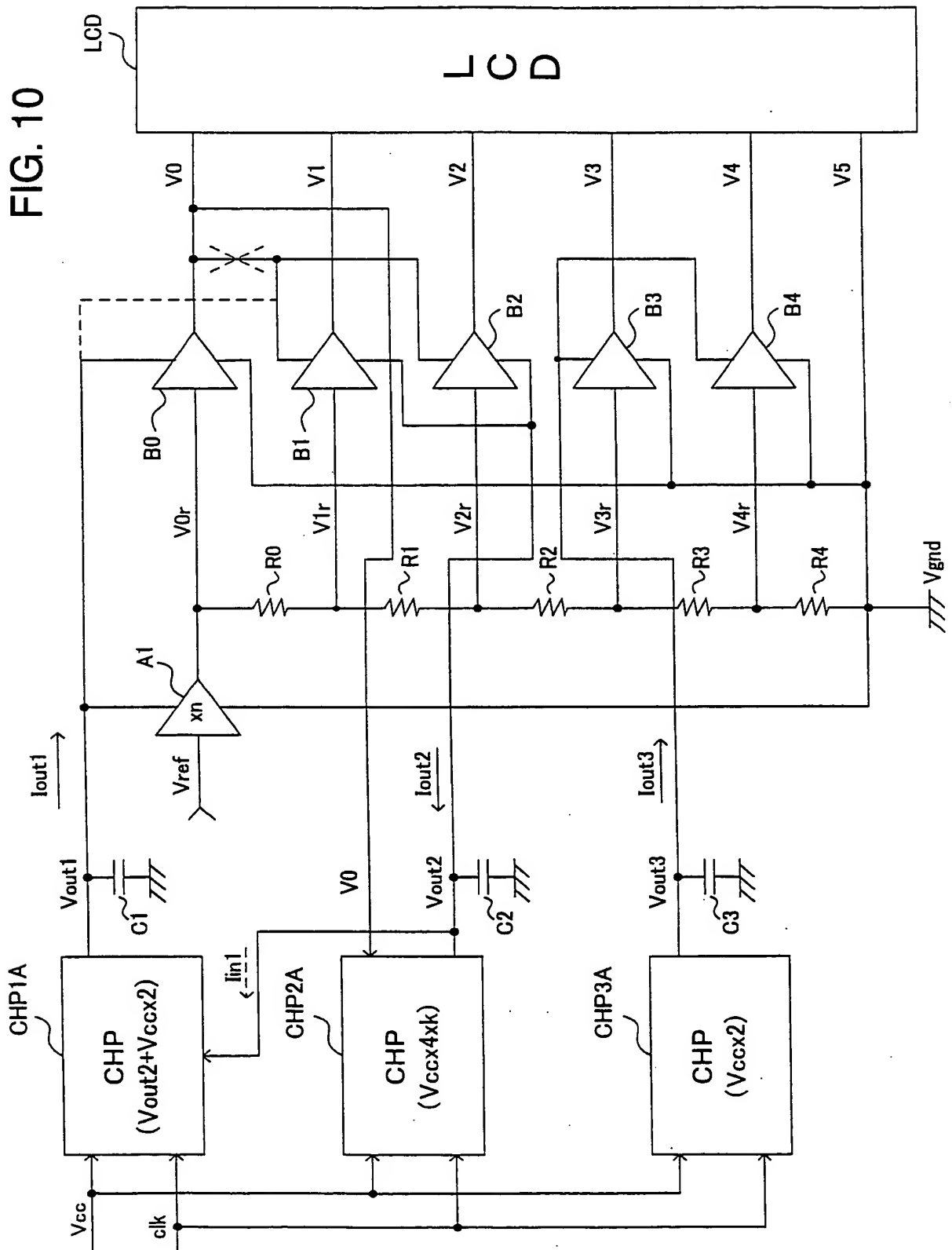


FIG. 11

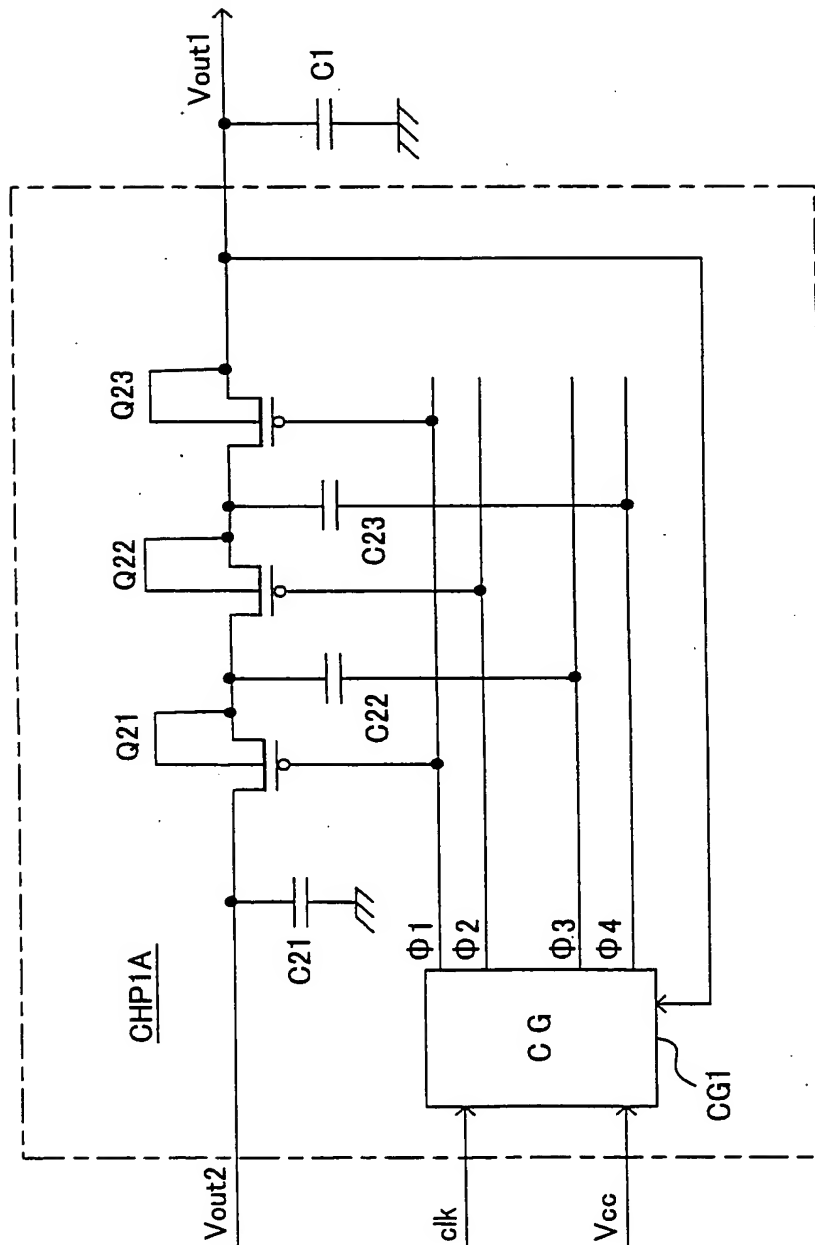


FIG. 12

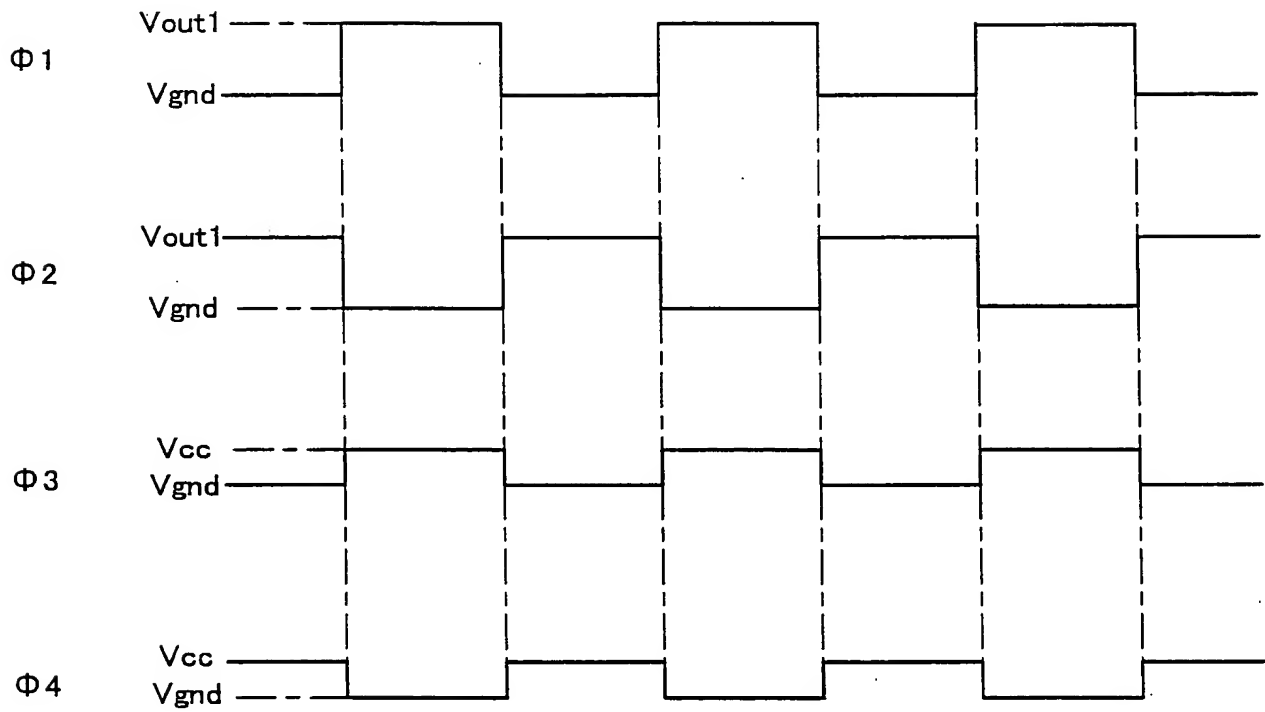


FIG. 13

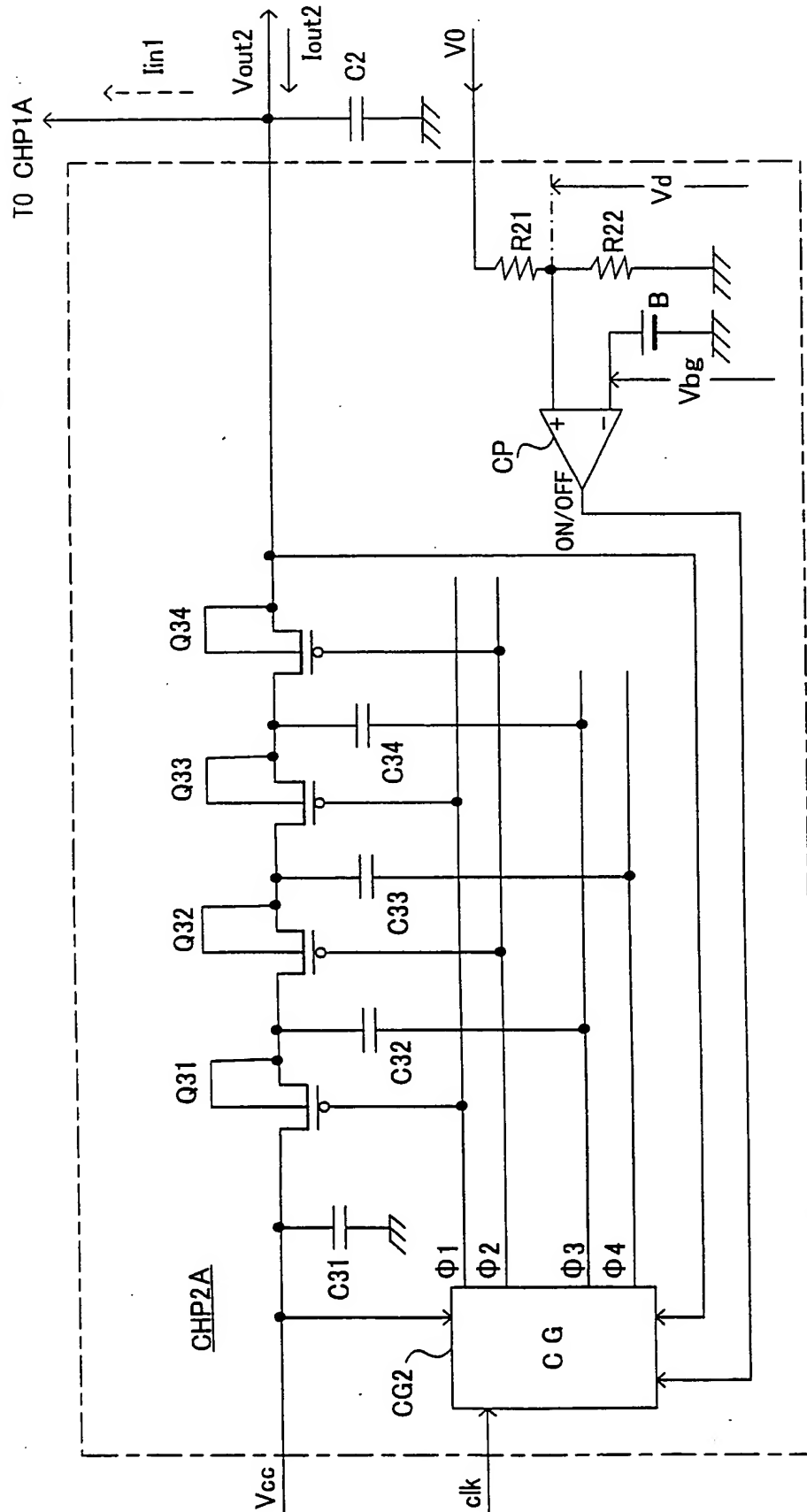
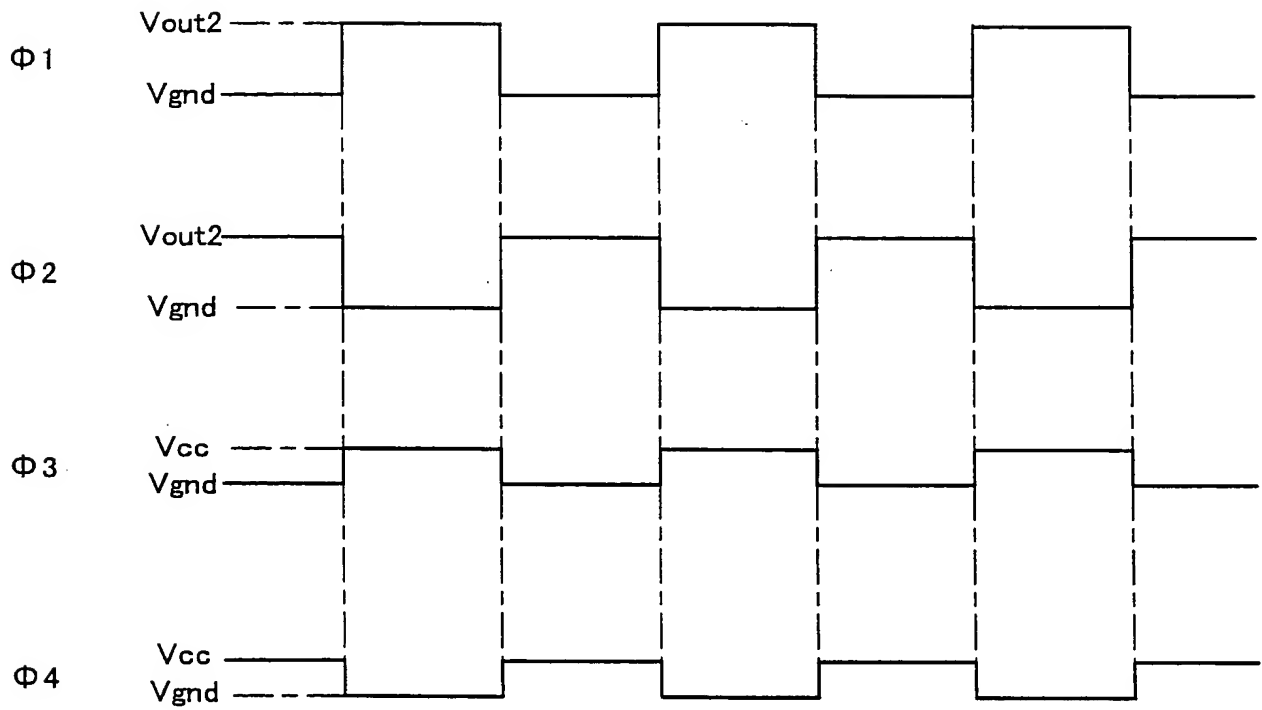


FIG. 14



PRIOR ART  
FIG. 15

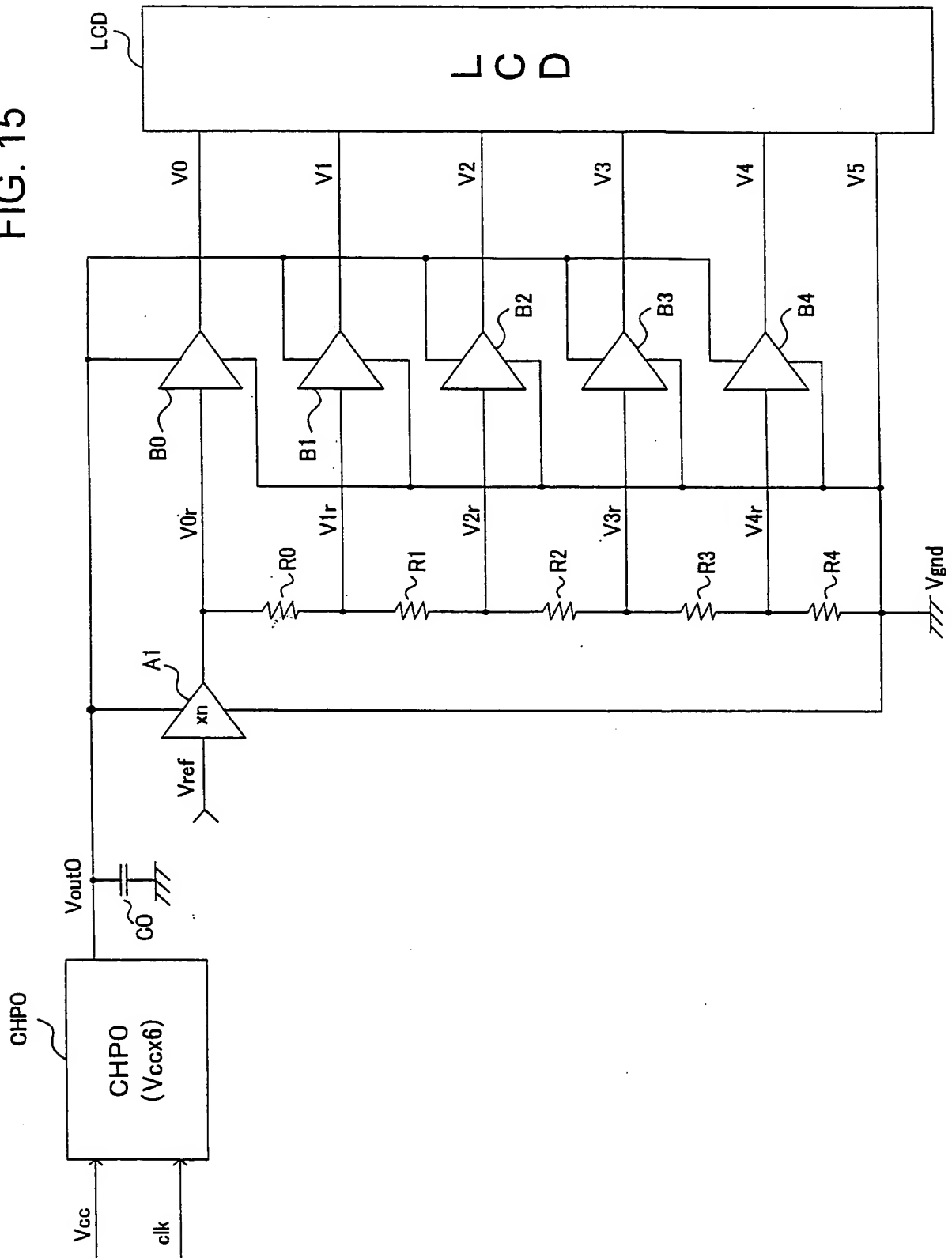


FIG. 16

